UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,334	01/26/2004	Syuichi Saito	107337-00056	7522

4372 7590 03/07/2006

ARENT FOX PLLC
1050 CONNECTICUT AVENUE, N.W.
SUITE 400
WASHINGTON, DC 20036

EXAMINER	
CHUNG, PHUNG M	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,334	SAITO, SYUICHI	
	Examiner	Art Unit	
	Phung My Chung	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, lines 1-3, the preamble of the claim is "A semiconductor testing circuit for performing a test of at least one of a write operation and a read operation of a semiconductor storage device", but there isn't any means or element that performing the test of at least one a write operation and a read operation of a semiconductor storage device in the body of the claim. Appropriate correction is required.

As per claims 2-9, these claims are also rejected because they dependent upon the rejected base claim.

As per claims 10 and 12, lines 3-22, "a self testing circuit for performing a test of at least one of a write opertion and a read operation of a semiconductor storage device, said self testing circuit includes, a plurality of counters..., and a switching circuit...is outputed" is not clear how the self testing circuit performing the test for at least one of the write and read operation of the semiconductor storage device.

As per claims 11, lines 3-5 and 10-23, "a self testing circuit which perform a test of at least one of a write opertion and a read operation of a semiconductor storage device, said self

testing circuit includes, a plurality of counters..., and a switching circuit...is outputed" is not clear how the self testing circuit performing the test for at least one of the write and read operation of the semiconductor storage device.

As per claims 13-14, these claims are also rejected because they dependent upon the rejected base claim.

As per claim 15, lines 1-3, the preamble of the claim is "A semiconductor testing method for performing a test of at least one of a write operation and a read operation of a semiconductor storage device", but there isn't any step for performing the test of at least one a write operation and a read operation of a semiconductor storage device in the body of the claim. Appropriate correction is required.

As per claims 16-18, these claims are also rejected because they dependent upon the rejected base claim.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-18 (as best understood) are rejected under 35 U.S.C. 103 (a) as being unpatentable over Lefebvre et al (4,873,666) in view of applicant admitted prior art (AAPA)..

As per claims 1-3, Lefebvre et al disclose a circuit, comprising: a plurality of counters (WRITE COUNTER-217 and READ COUNTER-218) which designate a plurality of different portions of an address signal used in the at least one of a write operation and a read operation, each of the plurality of different portions comprising one bit or plurality of succesive bits; and

a switching circuit (219) which selectively outputs counter-control signals for individually controlling operations of the plurality of counters, where each of the counter-control signals is one of a common counter-control signal commonly used for the plurality of counters and the most significant bit (MSB) of one of the plurality of portions outputed from a first one of the plurality of counters other than a second one of the plurality of counters for which each of the counter-control signal is outputted. (See Figs. 2-3, col. 3, lines 50-68 to col. 4, lines 1-3, and col. 5, lines 52-68 to col. 6, lines 1-22). Lefebvre et al do not disclose a semiconductor testing circuit for performing a test of at least one of a write operation and a read operation of a semiconductor storage device. However, AAPA discloses such a semiconductor testing circuit for performing a test of at least one of a write operation and a read operation of a semiconductor storage device (pg. 2, lines 23-27 to pg. 4, lines 1-5). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the semiconductor testing circuit for performing a test of at least one of a write operation and a read operation of the semiconductor storage device as taught by the AAPA into the invention of Lefebvre et al to perform a test of the write and read operation on the semiconductor storage device.

As per claim 4, the AAPA further discloses wherein a first one of the plurality of counters designates a column address of the semiconductor storage device, and a second one of the plurality of counters designates a row address of the semiconductor storage device. (See pg. 5, lines 1-6).

As per claims 5 and 7-8, Lefebvre et al further discloses wherein the first one of the plurality of counters is realized by a synchronous counter, and the second one of the plurality of counters is realized by an asynchronous counter. (See col. 3, lines 50-57).

As per claim 6, the AAPA further discloses wherein a third one of the plurality of counters designates a bank address of the semiconductor storage device (pg. 5, lines 1-6).

As per claim 9, the AAPA further discloses wherein the one of the plurality of portions designated by the one of the plurality of counters designates a bank address of the semiconductor storage device (pg. 5, lines 1-6).

As per claims 10-14, these claims are rejected under similar rationale as set forth in claims 1-3.

As per claims 15-18, these method claims are rejected under similar rationale as set forth in the system claims 1-3.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571- 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phung My Chung
Primary Patent Examiner